

**PATENT**

**Attorney Docket No.: 2207/12035**  
**ASSIGNEE: Intel Corporation**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

INVENTORS: Jason G. SANDRI et al.  
SERIAL NO: 10/001,961  
FILING DATE: December 5, 2001  
TITLE: METHOD AND APPARATUS FOR CONTROLLING ACCESS TO  
SHARED RESOURCES IN AN ENVIRONMENT WITH MULTIPLE  
LOGICAL PROCESSORS  
ART UNIT: 2195  
EXAMINER: Camquy TRUONG

**MAIL STOP RCE**  
COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, VA 22313-1450

**AMENDMENT AND REQUEST FOR CONTINUED**  
**EXAMINATION (RCE) UNDER 37 C.F.R. §1.114**

SIR:

The following amendments are associated with and accompanied by a Request for  
Continued Examination under 37 C.F.R. §1.114.

**A Listing of Claims** begin on page 2 of this paper.

**Remarks** begin on page 7 of this paper.

**Listing of Claims:**

1. (Currently Amended) A method comprising:

for a first logical processor, obtaining a lock on a semaphore controlling exclusive access to a resource descriptor, the resource descriptor describing a usage allocation of resources shared among a plurality of logical processors wherein the lock is obtained by a semaphore lock routine comprising writing an identifier of the logical processor and a lock value into a semaphore register;

obtaining exclusive access for said first logical processor to said resource descriptor if said lock is obtained;

determining which shared resources the first logical processor needs;

generating resource reservation data identifying the needed resource;

applying the resource reservation data to the resource descriptor;

querying said resource descriptor to determine whether resources needed by said first logical processor are available;

if resources needed by said first logical processor are available, updating said resource descriptor to reserve said resources for exclusive use by said first logical processor; and

releasing, utilizing a semaphore lock release routine to pass the identifier of the logical processor and a lock value, said exclusive access for said first logical processor to said resource descriptor.

2. (Original) The method of claim 1, further comprising:

if said resources needed by said first logical processor are not available, releasing said exclusive access for said first logical processor to said resource descriptor.

3. (Original) The method of claim 1, further comprising, after the releasing, accessing a shared resource by said first logical processor.

4. (Original) The method of claim 1, further comprising:

after exclusive access for said first logical processor to said resource descriptor is released, obtaining exclusive access for a second logical processor to said resource descriptor;  
querying said resource descriptor to determine whether resources needed by said second logical processor are available;  
if resources needed by said second logical processor are available, updating said resource descriptor to reserve said resources for the exclusive use of said second logical processor; and  
releasing said exclusive access for said second logical processor to said resource descriptor.

5. (Original) The method of claim 4 further comprising:

if said resources needed by said second logical processor are not available, releasing said exclusive access for said second logical processor to said resource descriptor.

6. - 9. (Canceled)

10. (Currently Amended) An apparatus comprising:

a plurality of logical processors to generate resource reservation data identifying ;  
a plurality of resources shared by said plurality of logical processors;

a resource descriptor to utilize said resource reservation data to identify a status of said  
shared resources; and

a semaphore comprising a semaphore register to reserve exclusive access for one of said  
plurality of logical processors to said resource descriptor, wherein a semaphore lock routine  
writes an identifier of one of the plurality of logical processors and a lock value into the  
semaphore register.

11. (Previously presented) The apparatus of claim 10, further comprising logic to:

cause a first logical processor to update said semaphore to reserve exclusive  
access to said resource descriptor;

cause said first logical processor to update said resource descriptor to reserve  
exclusive use of at least a first resource of said shared resources; and

subsequently cause said first logical processor to update said semaphore to release  
said exclusive access.

12. (Previously presented) The apparatus of claim 11, said logic to further:

cause a second logical processor to update said semaphore to reserve exclusive  
access to said resource descriptor;

cause said second logical processor to update said resource descriptor to reserve  
exclusive use of at least a second resource of said shared resources; and

subsequently cause said second logical processor to update said semaphore to  
release said exclusive access;

wherein after reserving exclusive use of said first and second resources, respectively, said first and second logical processors concurrently use said first and second resources, respectively.

13. (Currently Amended) A machine-readable medium storing instructions to perform a method comprising:

by a first logical processor,

utilizing a semaphore lock routine to write an identifier of the first logical processor and setting a lock bit in a semaphore register to reserve exclusive access to a resource descriptor register;

generating a first bitmap, said first bitmap comprising resource reservation data, and applying said resource reservation data to a resource descriptor to identify a first required resource;

applying said first bitmap to said resource descriptor register to reserve said first required resource;

re-setting, utilizing a semaphore lock release routine, said semaphore lock bit to release said exclusive access; and

using said first resource.

14. (Previously presented) The machine-readable medium of claim 13, said method further comprising:

by a second logical processor,

after said first logical processor has re-set said semaphore lock bit, setting said semaphore lock bit;

generating a second bitmap identifying a second required resource;

applying said second bitmap into said resource descriptor register to reserve said second required resource;

re-setting said semaphore lock bit to release said exclusive access; and

using said second resource;

wherein said first and second logical processors use said first and second resources in parallel.

15. (Previously presented) The machine-readable medium of claim 13, wherein said setting a lock bit comprises supplying an identifier of said first logical processor for writing into said semaphore register.

16. - 17. (Canceled)

18. (Currently Amended) A system comprising:

a plurality of logical processors to generate resource reservation data identifying;

a plurality of resources to be shared by said logical processors;

a resource descriptor utilize said resource reservation data to identify a status of said  
shared resources and to control access to said resources;

a semaphore register to reserve exclusive access for one of said plurality of logical processors to said resource descriptor to said resource descriptor, wherein a semaphore lock

routine is to write an identifier of one of the plurality of logical processors and a lock value into the semaphore register; and

access control logic to allocate one or more of said shared resources only when granted exclusive access to said resource descriptor by said semaphore register.

19. (Previously presented) The system of claim 18, wherein said resource descriptor includes a plurality of fields each to associate a resource with a logical processor identifier.

20. (Previously presented) The system of claim 18, wherein said access control logic is to

obtain a lock on said semaphore register to reserve exclusive access to said resource descriptor,

determine whether a needed resource is available based on said resource descriptor,

if so, reserve the resource, and

release the lock on the semaphore register.

21. (Previously presented) The system of claim 20, wherein said access control logic is further to reserve one or more resources by assigning a logical processor identifier to a corresponding resource.

22-23. (Cancelled).

24. (New) A system comprising:

a plurality of logical processors;

a plurality of resources to be shared by said logical processors;

a resource descriptor to control access to said resources;

a semaphore register to reserve exclusive access for one of said plurality of logical processors to said resource descriptor; and

access control logic to allocate one or more of said shared resources only when granted exclusive access to said resource descriptor by said semaphore register; and

unlock logic to prevent a failing logical processor from retaining a lock on the semaphore register, wherein the unlock logic includes causing a logical processor different from the failing logical processor to call a semaphore lock release routine and pass the routine the identifier of the failing logical processor.



**Remarks**

Claims 1-5, 10-15 and 18-23 are pending in the application. Claims 1, 10, 13, and 18 are amended. Reconsideration of the current rejection in light of the amendments is respectfully requested.

Furthermore, Applicants gratefully acknowledge the Office Action indication claim 23 contains allowable subject matter. *See* Office Action dated 5/29/2007, paragraph 28. New claim 24 incorporates all of the subject matter of allowable claim 23, including the base claim and intervening claims (*i.e.*, claim 22). Claims 22 and 23 are cancelled without prejudice or disclaimer.

**Claim rejections**

**Section 112, First Paragraph**

Claim 22 was rejected under 35 U.S.C. § 112, first paragraph as failing to satisfy the written description requirement. In particular, the Office Action objects to the language of the claim calling for preventing “a failing logical processor from retaining a lock on the semaphore register.” Attention is directed to paragraphs 0058-64 and Fig. 6, element 605, which clearly describes how a failed logical processor is prevented from retaining a lock on a semaphore register (e.g., by allowing a different logical processor to supply the failed logical processor’s LPID so as to release a lock on the semaphore register). In view of the above, the specification as filed provides a written description for the claim limitation. Accordingly, reconsideration and withdrawal of the rejection of claim 22 under 35 U.S.C. § 112, second paragraph is respectfully requested.

Section 103

Claims 1-5, 10-15, and 18-21 were rejected under 35 USC 103(a) as being unpatentable over Hays, Jr. et al. (US Patent No. 4,354,227) (“Hays”) in view of Forman et al. (US 5,544,353). Claim 22 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hays in view of Forman in further view of Lee et al. (US Patent No. 5,421,002) (“Lee”). The Applicant respectfully traverses the rejection. As discussed above, claim 22 is cancelled without prejudice or disclaimer. As such, the rejection of claim 22 is moot.

**Neither Hays nor Forman discloses the features of the claims.**

Looking at claim 1, for example, this claim sets forth a semaphore controlling exclusive access to a resource descriptor by a logical processor, and the resource descriptor being used to reserve resources for exclusive use by the logical processor. The cited references, taken singularly or in combination, fail to teach or suggest the semaphore and the resource descriptor as recited in this claim. Both Hays and Forman refer to a resource, and controlling access to the resource via a register value.

As to Hays, the Office Action states that the resource descriptor is shown at Col. 10, lines 9-14 and 22-28. In particular, the Office Action points to the “control register” that is recited in claim 1 of the Hays patent. This control register is used to control whether a processor can access a shared resource. Thus, at Col. 5, lines 32-37, Hays speaks of using a condition code register 24 to indicate whether the desired resource is available or not. In Hays (see, Col. 6, lines 3-11) a processor writes its ID to this register in one clock cycle in an effort to reserve the shared resource (e.g., a memory), and then checking in a later clock cycle for whether in fact the memory has been successfully reserved. As conceded in the Office Action, Hays fails to teach obtaining a lock on a semaphore controlling exclusive access to a resource descriptor, and

obtaining exclusive access for said first logical processor to the resource file, if the lock is obtained.

To make up for the deficiencies of Hays, the Office Action relies on Forman. The object of Forman is “to improve master process efficiency by reducing the length of time exclusive control over a master process indicator is required” (col. 2, lines 54-56). To this end, Forman relates to processes “‘racing’ for control of a resource” (col. 4, line 17). A process gets control of a resource by either creating or updating a shared control file, and becoming “master” of the control file. The invention of Forman purportedly achieves its object by removing the limitation that the master retain exclusive write access to the control file by “allowing the master to release the exclusive write mode while still being the master process for that resource.” See col. 4, lines 54-56. The Office Action specifically cites to Col. 6, lines 9-11 and 13, which again is citing to the claims of Forman. This particular section refers to requesting exclusive access to a file and waiting to try to gain exclusive access to the file. Such is repeated at Col. 5, lines 8-14.

In reviewing Hays and Forman, each reference individually refers to seeking exclusive access to a resource. In Hays, it is through access to a control register. Even assuming, *arguendo*, that Forman refers to a semaphore in Claim 1 or at Col. 5, lines 8-14 (the term is not used in Forman at all), such would be used to control access to a file. In each case, a semaphore or control register is used to control access between two devices to a shared resource. The present specification acknowledges that semaphores are used to control access to a shared resource (see para. 0009). The present specification and claims refer to providing a resource descriptor to reserve a shared resource for a logical processor and a semaphore controlling exclusive access to the resource descriptor. Both Hays and Forman only refer to one item to

control access to a shared resource and not the two levels of control present in the pending claims.

In view of the above, it is clear that neither Hays nor Forman contains any suggestion of multiple levels of control of a resource as in the present invention. Accordingly, the combination of Hays and Forman cannot yield the features of the claims. Moreover, there is no motivation for the combination of Hays and Forman, since they address different objects in different ways, and neither adds anything to the other in furtherance of their particular objects.

All of the independent claims recite elements for multiple levels of control. Claim 1 recites “obtaining a lock on a semaphore controlling exclusive access to a resource descriptor, the resource descriptor describing a usage allocation of resources shared among a plurality of logical processors” and “obtaining exclusive access for said first logical processor to said resource descriptor if said lock is obtained.” Independent claim 10 recites “a resource descriptor to identify a status of said shared resources; and a semaphore to reserve exclusive access for one of said plurality of logical processors to said resource descriptor.” Independent claim 13 recites “setting a lock bit in a semaphore register to reserve exclusive access to a resource descriptor register” and “applying said first bitmap to said resource descriptor register to reserve said first required resource.” Independent claim 18 recites “a resource descriptor to control access to said resources” and “a semaphore register to reserve exclusive access for one of said plurality of logical processors to said resource descriptor.”

The recent Office Action asserts that Forman teaches a shared control file used to write identifying data including the master identity and a timestamp, citing column 5, lines 3-5. It further asserts this shared control file is a resource descriptor. *See* Office Action 5/29/2007, page 11. Applicants disagree.

The cited section states: “The process starts when a processor requests a common resource 150. The existence of a shared control file is tested 152. If no shared control file exists, the process creates one 154, obtains exclusive access, and writes identifying data including the master identity and a timestamp 180.” It describes a process including a request of a *single* common resource 150. It then describes testing to determine the existence of a shared control file related to the single common resource 150. If no such shared control file relating to that common resource 150 exists, the described process creates one, obtains exclusive access, and writes identifying data to the shared control file.

Applicants submit the cited section including the description of a temporary shared control file dedicated only to a *single* commonly-shared resource is not the same as a resource descriptor, the resource descriptor describing a usage allocation of resources shared among a plurality of logical processors (*e.g.*, as described in claim 1).

The description of Forman confirms that the shared control file does not relate to usage allocation of among resources, but rather is dedicated only to a single “common resource”. *See e.g.*, Abstract, Summary of the Invention, and column 4, lines 15-20. The Forman reference, in multiple places (including the cited section discussed immediately above), describes the creation of the cited temporary shared control file dedicated to a single shared resource that is discarded in favor of a new one when the old one becomes “stale”. *See e.g.*, column 5, line 23. Clearly, this is not the same as a resource descriptor that describes *usage allocation* amongst various resources. Indeed, the cited shared control file does not relate to usage allocation amongst various resources at all. As such, Applicants submit the current rejection is lacking and should be withdrawn.

Lee fails to make up for the deficiencies of Hays and Forman. Lee refers to redundant busses and does not in any way teach or suggest the multiple levels of controlling access to a resource as recited in each of the pending claims.

In view of the above, withdrawal of the asserted rejection is respectfully requested.

**Conclusion**

In light of the above discussion, Applicant respectfully submits that the present application is in all aspects in allowable condition, and earnestly solicits favorable reconsideration and early issuance of a Notice of Allowance.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application. The Office is authorized to charge any fees related to this communication to Deposit Account No. 11-0600.

Respectfully submitted,  
KENYON & KENYON LLP

Dated: October 31, 2007

By: Sumit Bhattacharya/  
Sumit Bhattacharya  
Reg. No. 51,469

KENYON & KENYON LLP  
333 West San Carlos Street  
Suite 600  
San Jose, California 95110  
Tel: (408) 975-7500  
Fax: (408) 975-7501

111090.1